

Appl. No. 09/473,575

Amdt. dated April 7, 2004

Reply to Office Action of February 12, 2004

REMARKS

This Amendment is in response to the Office Action mailed February 12, 2004. In the Office Action, the Examiner rejected claims 63, 65, 67-70, 85-90, and 92-97 under 35 U.S.C. § 112, rejected claims 62-70 under 35 U.S.C. § 102, and rejected. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

1. Claims 62, 63, 65, 67-70 and 84-97 remain pending in this application.

Rejection Under 35 U.S.C. § 112

3. The Examiner rejects claims 63, 65, 67-70, 85-90, and 92-97 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 63 has been amended to provide antecedent basis for the elements noted by the Examiner.

5. Claim 65 has been amended to provide antecedent basis for the elements noted by the Examiner.

6. Claim 68 has been amended to provide antecedent basis for the element noted by the Examiner.

7. Claim 85 has been amended to provide antecedent basis for the elements noted by the Examiner.

8. Claim 86 has been amended to provide antecedent basis for the elements noted by the Examiner.

9. Claim 88 has been amended to provide antecedent basis for the element noted by the Examiner.

10. Claim 92 has been amended to provide antecedent basis for the elements noted by the Examiner.

11. Claim 93 has been amended to provide antecedent basis for the elements noted by the Examiner.

12. Claim 95 has been amended to provide antecedent basis for the element noted by the Examiner.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 63, 65, 67-70, 85-90, and 92-97 under 35 U.S.C. § 112, second paragraph.

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Rejections Under 35 U.S.C. § 102

14. The Examiner rejects claims 62, 63, 84-85, and 91-92 under 35 U.S.C. § 102(e) as being anticipated by Prigge (US 5,623,471).

The Examiner provides no specific statement of how the specific claim language reads on the cited portions of Prigge. Applicant has carefully reviewed the cited disclosure of Prigge and is unable to identify anything that even remotely appears to disclose performing allocation in a resource based upon the current processing mode. Applicant respectfully requests that the Examiner explain with more specificity how Prigge discloses these elements of the claimed invention if the Examiner intends to maintain this rejection.

15. Regarding claim 84, the Examiner asserts that Prigge discloses:

fetching instructions from one or more threads based upon a current processing mode (col. 3, lines 27-57, figs. 2-4); and,

performing allocation in a resource for the instructions based upon the current processing mode (col. 2, lines 4-9, col. 3, lines 20-31, figs. 2-4).

Prigge discloses an adaptive backup for storage library that uses two available recording devices when available. This is entirely unlike the present invention which is directed to allocating the resources required by a processor to execute instructions. Applicant has amended claim 84 to clarify this distinction based *inter alia* in the specification as filed at page 15, lines 8-20.

16. Regarding claim 85, the Examiner asserts that Prigge further discloses:

assigning the entire resource to the thread that is active if the current processing mode is single threading (fig. 3, fig. 4, 402, 404), and,

assigning a portion of the resource to each of the threads running concurrently if the current processing mode is multithreading (fig. 3, fig. 4, 402, 424).

Prigge discloses allocation of buffers based on the availability of recording devices. This is entirely unlike the allocating of processor resources of the present invention. Applicant has amended claims 84-86 to clarify that *processor* resources are allocated as disclosed *inter alia* in the specification as filed at page 16, lines 4-7.

17. The Examiner rejects claims 62-63 and 91-92 on the same ground as stated in claims 84-85. Applicant likewise traverses the rejection of claims 62-63 and 91-92 on the same ground as stated in claims 84-85. Claims 62-63, 65, and 91-93 have been amended similarly to claims 84-86. Further, applicant respectfully points out that claims 62-63 are apparatus claims directed to a processor and contain the elements of "an instruction delivery engine" and "an allocator." Applicant is unable to find any disclosure of such elements in Prigge.

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Applicant respectfully requests that the Examiner withdraw the rejection of claims 62, 63, 84-85, and 91-92 under 35 U.S.C. § 102(e) as being anticipated by Prigge.

Rejection Under 35 U.S.C. § 103

19. The Examiner rejects claims 65, 67-70, 86-90, and 93-97 under 35 U.S.C. § 103(a) as being unpatentable over Prigge (US 5,623,471) as applied to claims 84-85 above, in view of Levy et al. (US 2001/0004755).

20. Regarding claim 86, the Examiner admits that Prigge fails to teach the additional elements as claimed. The Examiner asserts that Levy teaches:

allocating an amount of entries for the instructions from each respective thread in the respective portion if the respective portion has sufficient available entries ([0074], [0084], [0089], and [0140]), and

activating at least one stall signal if the respective portion does not have sufficient available entries ([0084], [0120], and page 8 table 3).

The Examiner fails to make any argument with regard to these elements of claim 86:

if the current processing mode is single threading,

allocating an amount of entries for the instructions from the active thread in the resource if the resource has sufficient available entries, and

activating at least one stall signal if the resource does not have sufficient available entries; and,

if the current processing mode is multithreading,

Applicant assumes that the Examiner considers the teaching of Prigge [0089] that "FSR can concentrate all of its register resources on a solitary thread, when only one thread is running" to teach or suggest the undiscussed elements of claim 86. Applicant respectfully disagrees with any such conclusion. The execution of one thread in multithreading mode is not the same as execution in single threading mode. Indeed, as stated by Prigge [0089] "a concern about multithreaded architectures ... [is] their (possibly reduced) performance when only a single thread is executing." The processor performance is not the same for execution of a single thread in multithreading mode and execution in single threading mode. The present invention addresses this concern by providing a processor that can operate in either single threading mode or multithreading mode and providing resource allocation that is responsive to the threading mode. Neither Prigge or Levy, alone or in combination, teach or suggest a processor with more than one threading mode and resource allocation that is dependent on the threading mode.

21. Regarding claim 87, the Examiner asserts that Levy teaches instruction stalling generally as a condition that can occur in a processor and when there is insufficient resource available for performing function of the current threads ([0084], [0120], and page 8 table 3). Applicant respectfully disagrees. Applicant understands the cited portions of Levy to disclose instruction fetch stalling generally as a condition that can occur in a processor. However, nothing in Levy

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discloses an instruction delivery engine using a stall signal activated by an allocator to perform the instruction delivery engine's corresponding function.

Regarding claim 89, applicant finds nothing in the cited portions of Levy that discloses fetching an instruction from another thread if there is a stall.

22. Regarding claim 88, the Examiner asserts that Levy teaches instruction stalling generally as a condition that can occur in a processor and when there is insufficient resource available for performing function of the current threads ([0084], [0120], and page 8 table 3). Applicant respectfully disagrees. Applicant understands the cited portions of Levy to disclose replaying instructions on an exception in speculative execution of branches and to separately disclose instruction fetch stalling generally as a condition that can occur in a processor. However, nothing in Levy discloses refetching stalled instructions.

23. Regarding claim 90, the Examiner asserts that Levy teaches instruction stalling generally as a condition that can occur in a processor and when there is insufficient resource available for performing function of the current threads ([0084], [0120], and page 8 table 3). Applicant respectfully disagrees. Applicant finds nothing in the cited portions of Levy that discloses fetching an invalid instruction if there is a stall.

24. The Examiner rejects claims 65, 67-70, and 93-97 on the same ground as stated in claims 86-90. Applicant likewise traverses the rejection of claims 65, 67-70, and 93-97 on the same ground as stated in claims 86-90.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 65, 67-70, 86-90, and 93-97 under 35 U.S.C. § 103(a) as being unpatentable over Prigge in view of Levy.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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